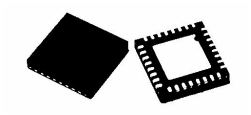
LNBH24L

Dual LNBS supply and control IC with step-up and I²C interface

Features

- Complete interface between LNBS and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93%@0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receivers output voltage specification
- Auxiliary modulation input (EXTM) facilitates DiSEqC™ 1.X encoding
- Low-drop post regulator and high efficiency step-up PWM with integrated power N-MOS allow low power losses
- Overload and over-temperature internal protections with I²C diagnostic bits
- Output voltage and output current level diagnostic feedback by I²C bits
- LNB short circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins



QFN32 5 x 5 mm (ePad)

Description

Intended for analog and digital DUAL satellite receivers/Sat-TV, Sat-PC cards, the LNBH24L is a monolithic voltage regulator and interface IC, assembled in QFN 5x5 ePAD, specifically designed to provide the 13 / 18 V power supply and the 22 kHz tone signaling for two independent LNB down-converters in the antenna dishes and/or multi-switch box. In this application field, it offers a dual tuner STBs complete solution with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

Table 1. Device summary

Order code	Package	Packaging
LNBH24LQTR	QFN32 5 x 5 (Exposed pad)	Tape and reel

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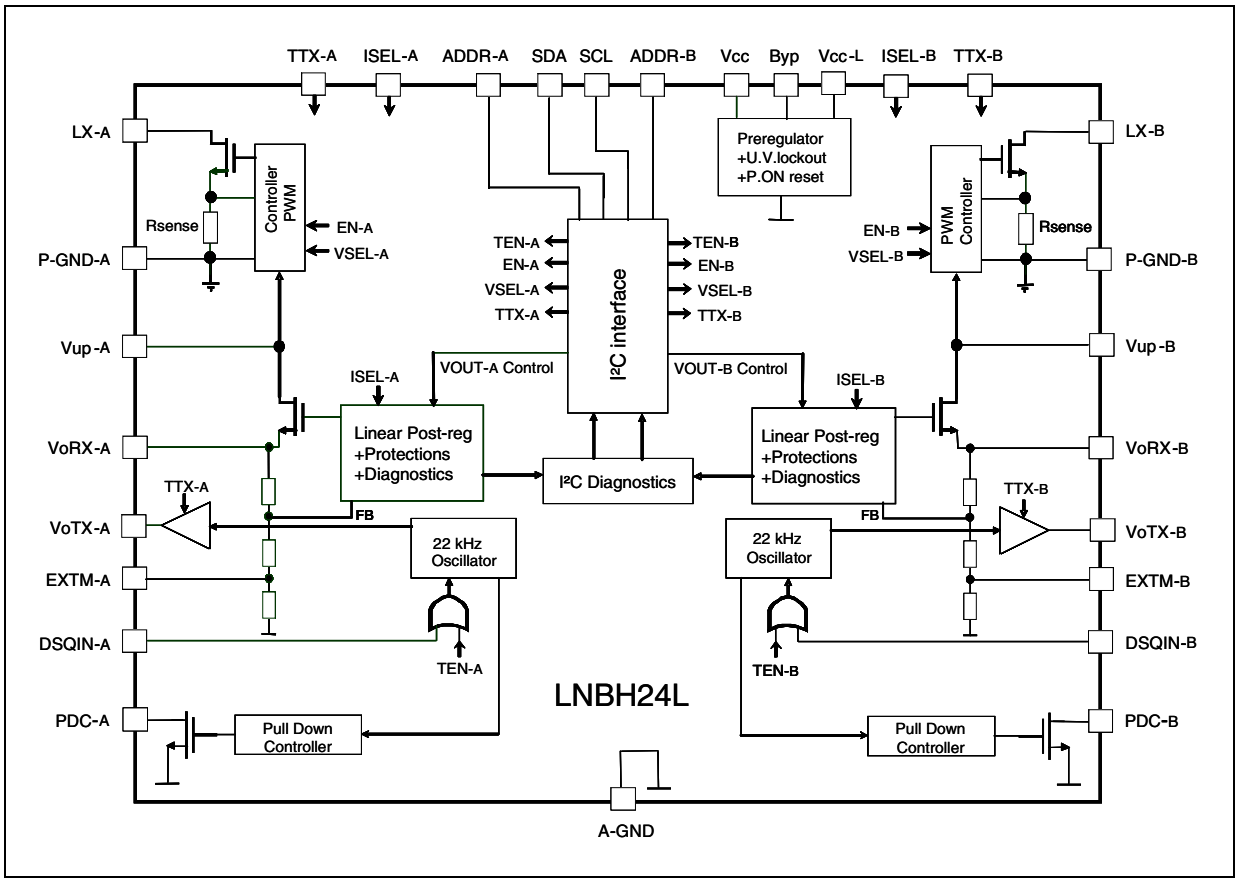
1 Block diagram

Figure 1. Block diagram



2 Introduction

The LNBH24L includes two completely independent sections. Unless for the V_{CC} and I²C inputs, each circuit can be separately controlled and have its independent external components. All the below specification must be considered equal for both sections (A/B).

2.1 Application information (valid for each section A/B)

This IC has a built-in DC-DC step-up converter that, from a single source from 8 V to 15 V, generates the voltages (V_{UP}) that let the linear post-regulator to work at a minimum dissipated power of 0.55 W typ. @ 500 mA load per channel (the linear post-regulator drop voltage is internally kept at V_{UP} - V_{OUT} = 1.1 V typ.). An under voltage lockout circuit will disable the whole circuit when the supplied V_{CC} drops below a fixed threshold (6.7 V typically).

Note: In this document the V_{OUT} is intended as the voltage present at the linear post-regulator output (V_{oRX} pin).

2.2 DiSEqC™ data encoding

The new internal 22 kHz tone generator is factory trimmed in accordance to the standards, and can be selected by I²C interface TTX bit (or TTX pin) and activated by a dedicated pin (DSQIN) that allows immediate DiSEqC™ data encoding, or through TEN I²C bit in case the 22 kHz presence is requested in continuous mode. In stand-by condition (EN bit LOW) the TTX function must be disabled setting TTX to LOW.

2.3 DiSEqC™ 1.X implementation by EXTM pin

In order to improve design flexibility and reduce the total application cost, an analogic modulation input pin is available (EXTM) to generate the 22 kHz tone superimposed to the V_{oRX} DC output voltage. An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. If the EXTM solution is used the output R-L filter can be removed (see *Section 5: Application circuits*) saving the external components cost.The pin EXTM modulates the V_{oRX} voltage through the series decoupling capacitor, so that:

$$V_{oRX(AC)} = V_{EXTM(AC)} \times G_{EXTM}$$

Where V_{oRX}(AC) and V_{EXTM}(AC) are, respectively, the peak to peak voltage on the V_{oRX} and EXTM pins while G_{EXTM} is the voltage gain from EXTM to V_{oRX}.

2.4 DISEQC™ 1.X implementation with V_{oTX} and EXTM pin connection

If an external 22 kHz tone source is not available, it is possible to use the internal 22 kHz tone generator signal available through the V_{oTX} pin to drive the EXTM pin. By this way the

V_{oTX} 22 kHz signal will be superimposed to the V_{oRX} DC voltage to generate the LNB output 22 kHz tone (see *Figure 3: LNBH24L with internal tone for DiSEqC 1.X applications*). The internal 22 kHz tone generator available through the V_{oTX} pin must be activated during the 22 kHz transmission by DSQIN pin or by the TEN bit.The DSQIN internal circuit activates the 22 kHz tone on the V_{oTX} output with 0.5 cycles ± 25 µs delay from the TTL signal presence on the DSQIN pin, and it stops with 1 cycles ± 25 µs delay after the TTL signal is expired. The V_{oTX} pin internal circuit must be preventively set ON by the TTX function. This can be controlled both through the TTX pin and by I²C bit. As soon as the tone transmission is expired, the V_{oTX} must be disabled by setting the TTX to LOW. The 13 / 18 V power supply is always provided to the LNB from the V_{oRX} pin.

2.5 PDC optional circuit for DISEQC™ 1.X applications using V_{oTX} signal on to EXTM pin

In some applications, at light output current (< 50 mA) and in case of heavy output capacitive load, the 22 kHz tone can be distorted. In this case it is possible to add the "Optional" external components shown in the typical application circuit (see *Figure 4: DiSEqC 1.x using external 22 kHz tone generator source through EXTM pin*) connected between V_{oRX} and PDC pin. This optional circuit acts as an active pull-down discharging the output capacitance only when the internal 22 kHz tone is activated.

2.6 I²C interface

The main functions of the IC are controlled via I²C bus by writing 6 bits on the system register (SR 8 bits in write mode). On the same register there are 5 bits that can be read back (SR 8 bits in read mode) to provide the diagnostic flags of two internal monitoring functions (OTF, OLF) and three output voltage register status (EN, VSEL, LLC) received by the IC (see *Section 2.8: Diagnostic and protection functions*). In read mode there are 3 test bits (TEST1-2-3) that must be disregarded from the MCU. While, in write mode, there 2 Test bits (TEST4-5) that must be always set LOW. Each section (A/B) has two selectable I²C addresses selectable respectively, by the ADDR-A and ADDR-B pins (see *Table 11: Address pins characteristics*).

2.7 Output voltage selection

When the IC sections are in stand-by mode (EN bit LOW), the power blocks are disabled. When the regulator blocks are active (EN bit HIGH), the output can be logic controlled to be 13 or 18 V by mean of the VSEL bit (voltage SELect) for remote controlling of non-DiSEqC LNBs. Additionally, the LNBH24L is provided with the LLC I²C bit that increase the selected voltage value to compensate possible voltage drop along the output line. In stand-by condition (EN bit LOW) all the I²C bits and the TTX pin must be set LOW (if the TTX pin is not used it can be left floating but the TTX bit must be set LOW during the stand-by condition).

2.8 Diagnostic and protection functions

The LNBH24L has two diagnostic internal functions provided via I²C bus by reading 2 bits on the system register (SR bits in read mode). The diagnostic bits are, in normal operation (no

failure detected), set to LOW. The diagnostic bits are dedicated to the over-temperature and over-load protections status (OTF and OLF).

2.9 Over-current and short circuit protection and diagnostic

In order to reduce the total power dissipation during an overload or a short circuit condition, the device is provided with a dynamic short circuit protection. It is possible to set the short circuit current protection either statically (simple current clamp) or dynamically by the PCL bit of the I²C SR. When the PCL (pulsed current limiting) bit is set lo LOW, the over current protection circuit works dynamically: as soon as an overload is detected, the output is shut-down for a time T_{OFF}, typically 900 ms. Simultaneously the diagnostic OLF I²C bit of the system register is set to "1". After this time has elapsed, the output is resumed for a time T_{ON} = 1/10 T_{OFF} = 90 ms (typ.). At the end of T_{ON}, if the overload is still detected, the protection circuit will cycle again through T_{OFF} and T_{ON}. At the end of a full T_{ON} in which no overload is detected, normal operation is resumed and the OLF diagnostic bit is reset to LOW. Typical T_{ON} + T_{OFF} time is 990 ms and an internal timer determines it. This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start-up in most conditions. However, there could be some cases in which a highly capacitive load on the output may cause a difficult start-up when the dynamic protection is chosen. This can be solved by initiating any power start-up in static mode (PCL=1) and, then, switching to the dynamic mode (PCL=0) after a chosen amount of time depending on the output capacitance. When in static mode, the diagnostic OLF bit goes to "1" when the current clamp limit is reached and returns LOW when the overload condition is cleared.

2.10 Thermal protection and diagnostic

The LNBH24L is also protected against overheating: when the junction temperature exceeds 150°C (typ.), the step-up converter and the liner regulator are shut-off, and the diagnostic OTF SR bit is set to "1". Normal operation is resumed and the OTF bit is reset to LOW when the junction is cooled down to 135°C (typ.)

2.11 Output current limit selection

The linear regulator current limit threshold can be set by an external resistor connected to ISEL pin. The resistor value defines the output current limit by the equation:

Equation 1

$$I_{MAX}\ [A] = \frac{10000}{R_{SEL}}$$

where R_{SEL} is the resistor connected between I_{SEL} and GND (see R2 in the typical application circuit). The highest selectable current limit threshold is 0.9 A typ. with R_{SEL}= 11 kΩ. The above equation defines the typical threshold value for each output. However, it is suggestible to not exceed for a long period a total amount of current of 1 A from both sections (I_{OUT_A} + I_{OUT_B} < 1 A) in order to avoid the over temperature protection triggering.

Note: External components are needed to comply to bidirectional DiSEqC™ bus hardware requirements. Full compliance of the whole application with DiSEqC™ specifications is not implied by the bare use of this IC. NOTICE: DiSEqC™ is a trademark of EUTELSAT.

3 Pin configuration

Figure 2. Pin connections (bottom view)

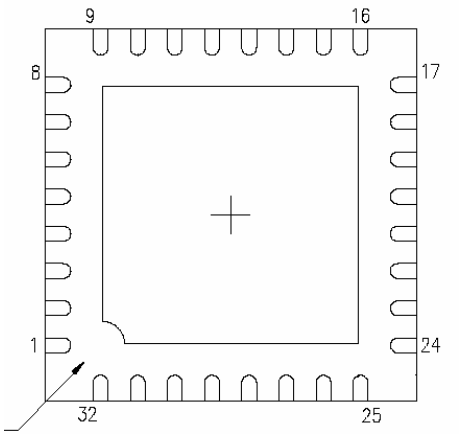


Table 2. Pin description

Pin n° (sec. A/B)	Symbol	Name	Pin function
21	V_{CC}	Supply Input	8 to 15 V IC DC-DC power supply.
20	V_{CC}_L	Supply Input	8 to 15 V analog power supply.
5 / 2	LX-A / LX-B	N-MOS Drain	Integrated N-channel Power MOSFETs drain.
16 / 25	V_{UP}-A / V_{UP}-B	Step-Up Voltage	Input of the linear post-regulators. The voltage on these pins is monitored by the internal step-up controllers to keep a minimum dropout across the linear pass transistors.
18 / 23	V_{oRX}-A / V_{oRX}-B	LDO Output Port	Outputs of the integrated low drop linear regulators. See *Table 7* for voltage selections and description.
17 / 24	V_{oTX} _A / V_{oTX} _B	Output Port during 22KHz Tone TX	Tone outputs to the LNB. See *Table 7* for selection.
6	SDA	Serial Data	Bidirectional data from / to I²C bus.
7	SCL	Serial Clock	Clock from I²C bus.
10 / 31	DSQIN-A / DSQIN-B	DiSEqC Inputs	These pins will accept the DiSEqC code from the main microcontroller. The LNBH24L will uses this code to modulate the internally generated 22 kHz carrier. Set to ground if not used.
12 / 29	TTX-A / TTX-B	TTX Enable	These pins can be used, as well as the TTX I²C bits of the system register, to control the TTX function enable before to start the 22 kHz tone transmission. Set floating or to GND if not used.
11 / 30	Reserved	Reserved	To be connected to GND.
9 / 32	PDC – A / PDC – B	Pull Down Control	To be connected to the external NPN transistors base to reduce the 22 kHz tone distortion in case of heavy capacitive load at light output current. If not used they can be left floating.

Table 2. Pin description (continued)

Pin n° (sec. A/B)	Symbol	Name	Pin function
13 / 28	EXTM-A / EXTM-B	External Modulation	External modulation inputs act on V_{oRX} linear regulator outputs to superimpose an external 22 kHz signal. Need DC decoupling to the AC source. If not used they can be left floating.
4 / 3	P-GND-A / P-GND-B	Power Grounds	DC-DC converters power grounds.
Epad	Epad	Exposed Pad	To be connected with power grounds and to the ground layer through vias to dissipate the heat.
22	A-GND	Analog Grounds	Analog circuits grounds.
19	BYP	By-pass Capacitor	Needed for internal pre-regulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device.
8 / 1	ADDR-A / ADDR-B	Address Setting	Two I²C addresses available for each section by setting the Address pins voltage level. See address pin characteristics table.
15/ 26	ISEL-A / ISEL-B	Current selection	The resistors "R_{SEL}" connected between I_{SEL} and GND define the linear regulators current limit protection threshold by the equation: $I_{max(typ)} = 10000 / R_{SEL}$.
14 / 27	Reserved	Reserved	To be left floating. Do Not connect to GND.

4 Maximum ratings

Table 3. Absolute maximum ratings (valid for both sections A/B)

Symbol	Parameter	Value	Unit
V_{CC-L}, V_{CC}	DC power supply input voltage pins	-0.3 to 16	V
I_{OUT}	Output current	Internally limited	mA
V_{oRX}	DC output pin voltage	-0.3 to 25	V
V_{oTX}	Tone output pin voltage	-0.3 to 25	V
LX	LX input voltage	-0.3 to 25	V
V_{UP}	DC input voltage	-0.3 to 24	V
V_I	Logic input voltage (TTX, SDA, SCL, DSQIN, ADDR pins)	-0.3 to 7	V
V_{OH}	Logic high output voltage (PDC pin)	-0.3 to 7	V
V_{EXTM}	EXTM pin voltage	-0.3 to 2	V
V_{BYP}	Internal reference pin voltage (1)	-0.3 to 4.6	V
ISEL	Current selection pin voltage	-0.3 to 4.6	V
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Junction temperature range	-25 to 150	°C
ESD	ESD rating with human body model (HBM) for all pins unless 4, 21, 22	2	kV
	ESD rating with human body model (HBM) for pins 21, 22	4	
	ESD rating with human body model (HBM) for pin 4	0.6	

1. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to network ground terminal.

Table 4. Operating ratings

Symbol	Parameter	Value	Unit
V_{CC-L}, V_{CC}	DC power supply input voltage pins	8 to 15	V
T_J	Junction temperature range	0 to 125	°C

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	2	°C/W
R_{thJA}	Thermal resistance junction-ambient with device soldered on 2s2p PC board	35	°C/W

5 Application circuits

Figure 3. LNBH24L with internal tone for DiSEqC 1.X applications

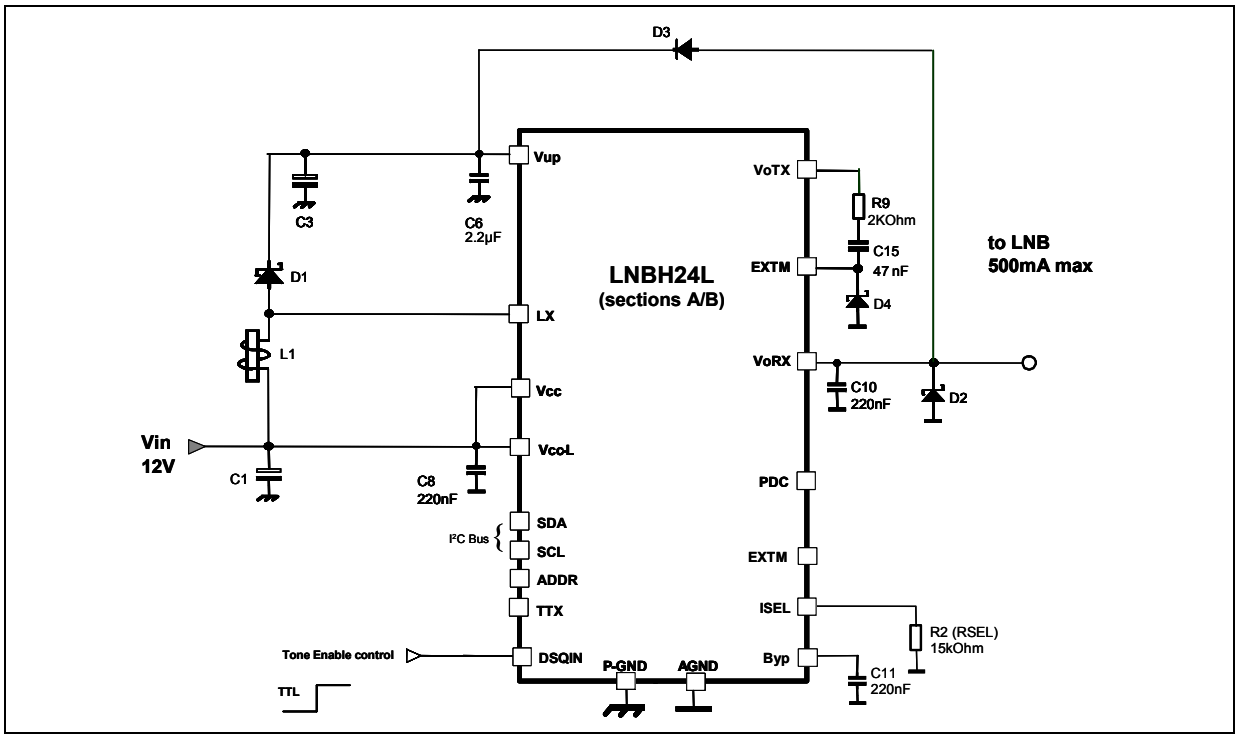


Figure 4. DiSEqC 1.x using external 22 kHz tone generator source through EXTM pin

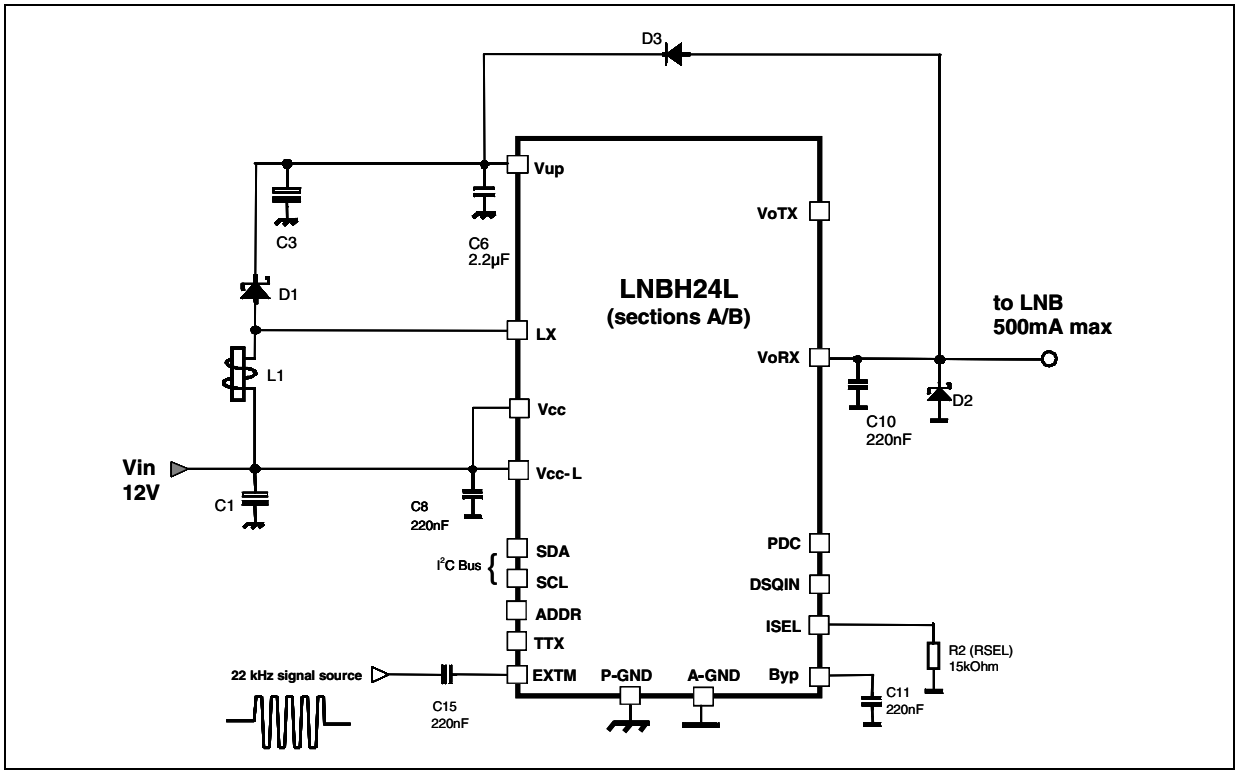


Figure 5. LNBH24L with PDC circuit for DiSEqC 1.X applications

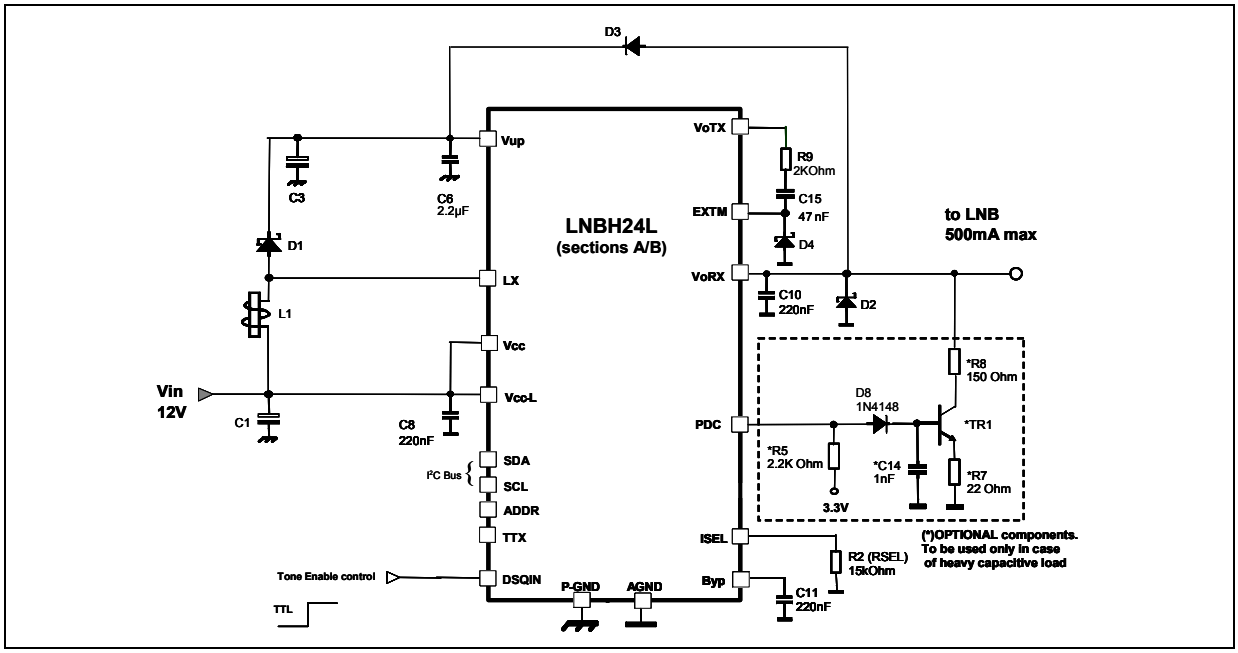


Table 6. Bill of material (valid for A and B sections unless for C1, C2, C7, C8 and C11)

Component	Notes
R2, R9, R5 (1)	1/16 W resistors. Refer to the typical application circuit for the relative values
R7 (1), R8 (1)	1/2 W resistors. Refer to the typical application circuit for the relative values
C1	25 V electrolytic capacitor, 100 µF or higher is suitable
C3	25 V, 220 µF electrolytic capacitor, ESR in the 100 mΩ to 350 mΩ range
C6, C8, C10, C11, C15, C14 (1)	25 V ceramic capacitors. Refer to the typ. appl. circuit for the relative values
D1	STPS130A or similar schottky diode with V_{RRM} > 25 V and I_F(AV) higher than: $I_{F(AV)} > I_{OUT_MAX} \times (V_{UP_MAX} / V_{IN_MIN})$
D2	STPS130A, 1N5818 or similar schottky diode with VRRM>25V. To be placed as close as possible to VoRX pin
D3	1N4001-07 or any similar general purpose rectifier
D4	BAT54, STPS130A, BAT43, 1N5818, or similar schottky diode with VRRM>20V. To be placed as close as possible to EXTM pin
D8	1N4148 or similar
TR1 (1)	BC817 or similar NPN general-purpose transistor
L1	22 µH inductor with $I_{sat} > I_{peak}$ where I_{peak} is the boost converter peak current: (see *Equation 2*)

1. These components can be added to avoid any 22 kHz tone distortion due to heavy capacitive output loads. If not needed they can be removed leaving the PDC pin floating.

Equation 2

$$I_{PEAK} = \frac{V_{UP_MAX} * I_{OUT_MAX}}{Eff * V_{IN_MIN}} + \frac{V_{IN_MIN}}{2LF}\left(1 - \frac{V_{IN_MIN}}{V_{UP_MAX}}\right)$$

6 I²C bus interface

Data transmission from main microprocessor to the LNBH24L and vice versa takes place through the 2 wires I²C bus interface, consisting of the 2 lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

6.1 Data validity

As shown in *Figure 6*, the data on the SDA line must be stable during the high semi-period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

6.2 Start and stop condition

As shown in *Figure 7* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

6.4 Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 8*). The peripheral (LNBH24L) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed has to generate acknowledge after the reception of each byte, otherwise the SDA line remain at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBH24L won't generate acknowledge if the V_{CC} supply is below the under-voltage lockout threshold (6.7 V typ.).

6.5 Transmission without acknowledge

Avoiding to detect the acknowledges of the LNBH24L, the microprocessor can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data. This approach of course is less protected from misworking and decreases the noise immunity.

Figure 6. Data validity on the I²C bus

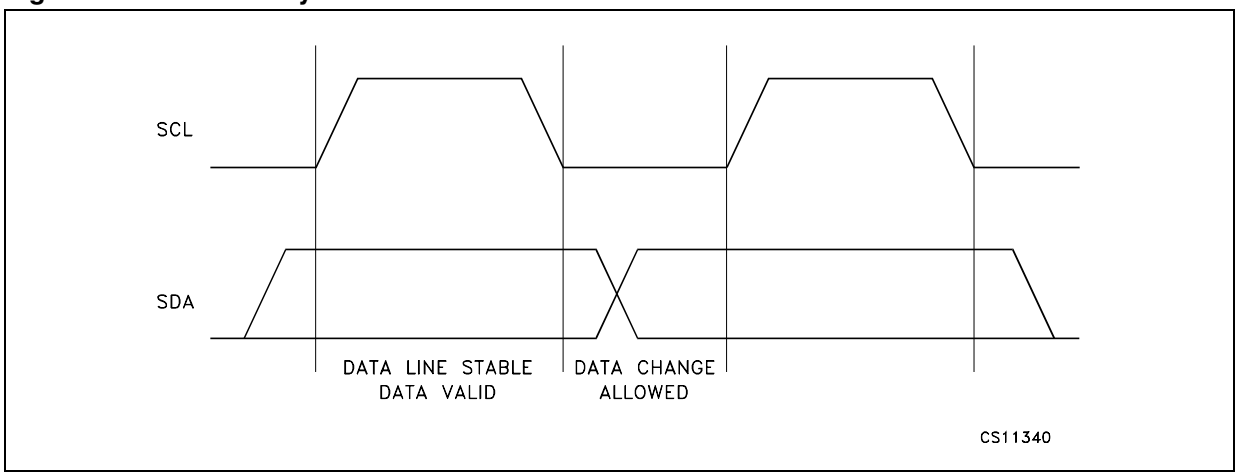


Figure 7. Timing diagram of I²C bus

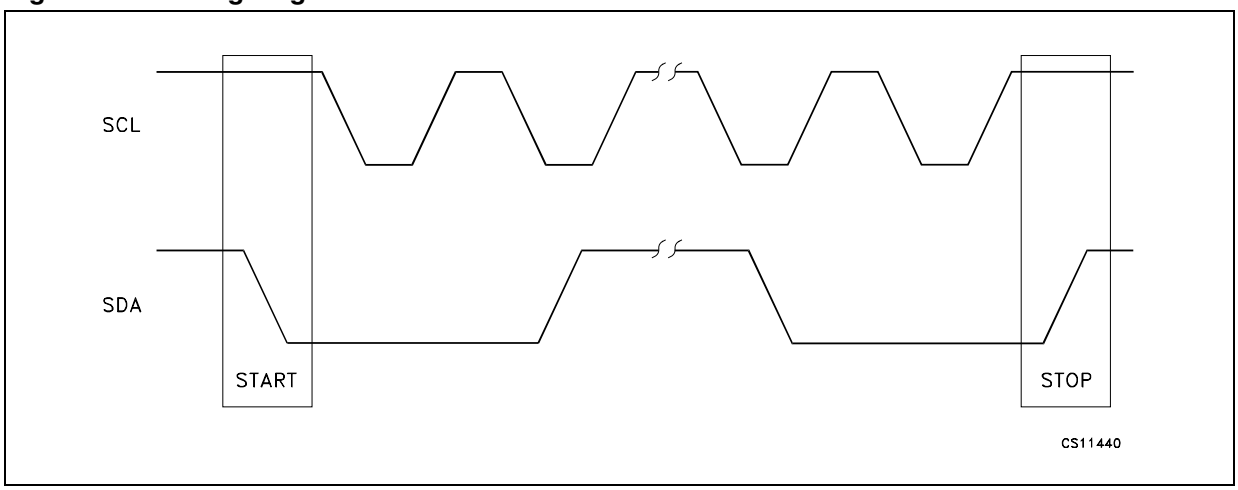
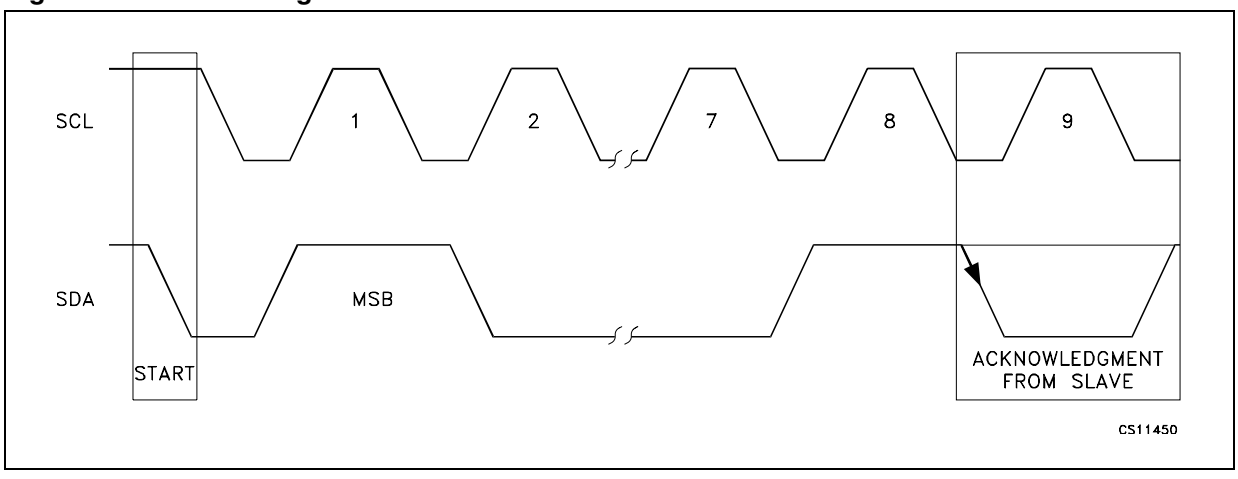


Figure 8. Acknowledge on the I²C bus



7 LNBH24 software description

The LNBH24L I²C interface controls both the IC sections A and B depending on the address sent before the DATA byte. All the below description is valid for both sections.

7.1 Interface protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte [the LSB bit determines read (=1)/write (=0) transmission]
- A sequence of data (1 byte + acknowledge)
- A stop condition (P)

	Section address (A or B)									Data									
	MSB							LSB		MSB							LSB		
S	0	0	0	1	0	X	X	R/W	ACK									ACK	P

ACK = Acknowledge

S = Start

P = Stop

R/W = 1/0, Read/Write bit

X = 0/1, two addresses for each section selectable by ADDR-A/B pins (see *Table 11*)

7.2 System register (SR, 1 Byte for each section A and B)

Mode	MSB							LSB
Write	PCL	TTX	TEN	LLC	VSEL	EN	TEST4	TEST5
Read	TEST1	TEST2	TEST3	LLC	VSEL	EN	OTF	OLF

Write = control bits functions in write mode

Read = diagnostic bits in read mode.

All bits reset to 0 at power on

7.3 Transmitted data (I²C bus write mode) for each sections A/B

When the R/W bit in the section address is set to 0, the main microprocessor can write on the system register (SR) of the relative section (A or B, depending on the 7 bit address value) via I²C bus. All and 8 bits are available and can be written by the microprocessor to control the device functions as per the below truth table (*Table 7*).

Table 7. Truth table

PCL	TTX	TEN	LLC	VSEL	EN	TEST4	TEST5	Function
	0		0	0	1	0	0	V_{oRX} = 13.3 V, V_{UP}=14.4 V, (V_{UP}-V_{oRX}=1.1 V typ.)
	0		0	1	1	0	0	V_{oRX} = 18.2 V, V_{UP}=19.3 V, (V_{UP}-V_{oRX}=1.1 V typ.)
	0		1	0	1	0	0	V_{oRX} = 14.3 V, V_{UP}=15.4 V, (V_{UP}-V_{oRX}=1.1 V typ.)
	0		1	1	1	0	0	V_{oRX} = 19.2 V, V_{UP}=20.3 V, (V_{UP}-V_{oRX}=1.1 V typ.)
	1	0			1	0	0	Internal 22 kHz controlled by DSQIN pin (only if TTX=1)
	1	1			1	0	0	Internal 22 kHz tone output on V_{oTX} is always activated
	0	0			1	0	0	Internal 22 kHz generator disabled, EXTM modulation enabled
	0				1	0	0	V_{oRX} output is ON, V_{oTX} Tone generator output is OFF
	1				1	0	0	V_{oRX} output is ON, V_{oTX} Tone generator output is ON
0					1	0	0	Pulsed (Dynamic) current limiting is selected
1					1	0	0	Static current limiting is selected
X	X	X	X	X	0	X	X	Power block disabled

X = don't care

Values are typical unless otherwise specified

Valid with TTX pin floating

7.4 Diagnostic received data (I²C read mode) for both sections A/B

The LNBH24L can provide to the MCU master a copy of the diagnostic system register information via I²C bus in read mode. The read mode is master activated by sending the chip address with R/W bit set to 1. At the following master generated clocks bits, LNBH24L issues a byte on the SDA data bus line (MSB transmitted first). At the ninth clock bit the master can:

- Acknowledge the reception, starting in this way the transmission of another byte from the LNBH24L
- No acknowledge, stopping the read mode communication

Three bits of the register are read back as a copy of the corresponding write output voltage register status (LLC, VSEL, EN), two bits convey diagnostic information about the over-temperature (OTF), output over-load (OLF) and three bit are for internal usage (TEST1-2-3) and must be disregarded by the MCU software. In normal operation the diagnostic bits are set to zero, while, if a failure is occurring, the corresponding bit is set to one. At start-up all the bits are reset to zero.

Table 8. Register

TEST1	TEST2	TEST3	LLC	VSEL	EN	OTF	OLF	Function
			These bits are read exactly the same as they were left after last write operation			0		T_J < 135°C, normal operation
						1		T_J > 150°C, power blocks disabled
							0	I_O < I_{OMAX}, normal operation
							1	I_O > I_{OMAX}, Overload Protection triggered
X	X	X						These bits status must be disregarded by the MCU.

X = don't care

Note: Values are typical unless otherwise specified.

7.5 Power-ON I²C interface reset

The I²C interface built in the LNBH24L is automatically reset at power-on. As long as the V_{CC} stays below the undervoltage lockout (UVL) threshold (6.7 V), the interface will not respond to any I²C command and the system registers (SR) are initialized to all zeroes, thus keeping the power blocks disabled. Once the V_{CC} rises above 7.3 V typ. The I²C interface becomes operative and the SRs can be configured by the main microprocessor. This is due to 500 mV of hysteresis provided in the UVL threshold to avoid false re-triggering of the Power-ON reset circuit.

7.6 Address pins

For each section of the LNBH24L it is possible to select two I²C interface addresses by means of the relevant ADDR pin. The ADDR pins are TTL compatible and can be set as per hereafter address pins characteristics see *Table 11*.

7.7 DiSEqC™ implementation for each section A/B

LNBH24L helps system designer to implement DiSEqC 1.x protocol by allowing an easy PWK modulation of the 22 kHz carrier through the EXTM and V_{oTX} pins. Full compliance of the system to the specification is thus not implied by the bare use of the LNBH24L (see DiSEqC 1.x operation descriptions and typical application circuits).

8 Electrical characteristics

Refer to the typical application circuits, T_J from 0 to 85 °C, EN=1, VSEL=LLC=TEN=PCL=TEST4=TEST5=TTX=0, R_{SEL}=15 kΩ, DSQIN=LOW, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25°C. V_{OUT} = V_{oRX} pin voltage. See software description section for I²C access to the system register.

Table 9. Electrical characteristics of each sections A/B

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage	I_{OUT} = 500 mA, VSEL = LLC = 1		8	12	15	V
I_{IN}	Supply current	Both sections A and B enabled I_{OUT} = 0			20	30	mA
		Both sections A and B enabled, optional PDC circuit not connected. EN = TEN = TTX = 1, I_{OUT} = 0			50	70	
		EN = 0			6		
V_{OUT}	Output voltage	VSEL = 1 I_{OUT} = 500 mA	LLC = 0	17.3	18.2	19	V
			LLC = 1		19.2		
V_{OUT}	Output voltage	VSEL = 0 I_{OUT} = 500 mA	LLC = 0	12.6	13.3	14	
			LLC = 1		14.3		
V_{OUT}	Line regulation	V_{IN} = 8 to 15 V	VSEL=0		5	40	mV
			VSEL=1		5	60	
V_{OUT}	Load regulation	VSEL=0 or 1, I_{OUT} from 50 to 500mA				200	
I_{MAX}	Output current limiting	RSEL= 15 kΩ		500		800	mA
		RSEL= 11 kΩ		750		1000	
I_{SC}	Output short circuit current	VSEL=0/1			800		mA
T_{OFF}	Dynamic overload protection OFF time	PCL=0, Output Shorted			900		ms
T_{ON}	Dynamic overload protection ON time	PCL=0, Output Shorted			T_{OFF}/ 10		
F_{TONE}	Tone frequency	DSQIN=HIGH or TEN=1, TTX=1		18	22	26	kHz
A_{TONE}	Tone amplitude using internal tone generator	DSQIN=HIGH or TEN=1, TTX=1, DiSEqC 1.X configuration using internal generator, C_{BUS} from 0 to 250 nF, I_{OUT} from 50 to 500 mA		0.4	0.650	0.9	V_{PP}
A_{TONE}	Tone amplitude using internal tone generator	DSQIN=HIGH or TEN=1, TTX=1, DiSEqC 1.X configuration using internal generator, I_{OUT} from 0 to 500 mA, C_{OUT} from 0 to 750 nF, PDC optional circuit connected to LNB bus(1)		0.4	0.650	0.9	V_{PP}
D_{TONE}	Internal tone duty cycle	DSQIN=HIGH or TEN=1, TTX=1 (using internal generator)		40	50	60	%

Table 9. Electrical characteristics of each sections A/B (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_r, t_f	Tone rise or Fall time	DSQIN=HIGH or TEN=1, TTX=1 (using internal generator)	5	8	15	µs
V_{PDC_OL}	PDC pin logic LOW	I_{PDC} = 2 mA		0.3		V
I_{PDC_OZ}	PDC pin leakage current	V_{PDC} = 5 V		1		µA
G_{EXTM}	External modulation Gain	ΔV_{OUT}/ ΔV_{EXTM}, freq. from 10 kHz to 50 kHz		1.8		
V_{EXTM}	External modulation input voltage	EXTM AC coupling (2)			400	mV_{PP}
Z_{EXTM}	External modulation impedance			2		kΩ
Eff_{DC-DC}	DC-DC converter efficiency	I_{OUT} = 500 mA		93		%
F_{SW}	DC-DC converter switching frequency			220		kHz
V_{IL}	DSQIN,TTX, pin logic low				0.8	V
V_{IH}	DSQIN,TTX, pin logic high		2			V
I_{IH}	DSQIN,TTX, pin input current	V_{IH} = 5 V		15		µA
I_{OBK}	Output backward current	EN = 0, V_{OBK} = 21 V		-6	-15	mA
T_{SHDN}	Thermal shut-down threshold			150		°C
ΔT_{SHDN}	Thermal shut-down hysteresis			15		°C

1. Guaranteed by design, but not tested in production
2. External signal maximum voltage for which the EXTM function is guaranteed

T_J from 0 to 85 °C, V_I = 12 V.

Table 10. I²C electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	LOW Level input voltage	SDA, SCL			0.8	V
V_{IH}	HIGH Level input voltage	SDA, SCL	2			V
I_{IN}	Input current	SDA, SCL, V_I = 0.4 to 4.5 V	-10		10	µA
V_{OL}	Low level output voltage	SDA (open drain), I_{OL} = 6 mA			0.6	V
F_{MAX}	Maximum clock frequency	SCL	400			kHz

T_J from 0 to 85 °C, V_I = 12 V.

Table 11. Address pins characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SECTION “A” ADDRESS SELECTION						
$V_{ADDR-A1}$	“0001000(R/W)” Address pin voltage range for section A	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
$V_{ADDR-A2}$	“0001001(R/W)” Address pin voltage range for section A	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V
SECTION “B” ADDRESS SELECTION						
$V_{ADDR-B1}$	“0001010(R/W)” Address pin voltage range for section B	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
$V_{ADDR-B2}$	“0001011(R/W)” Address pin voltage range for section B	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
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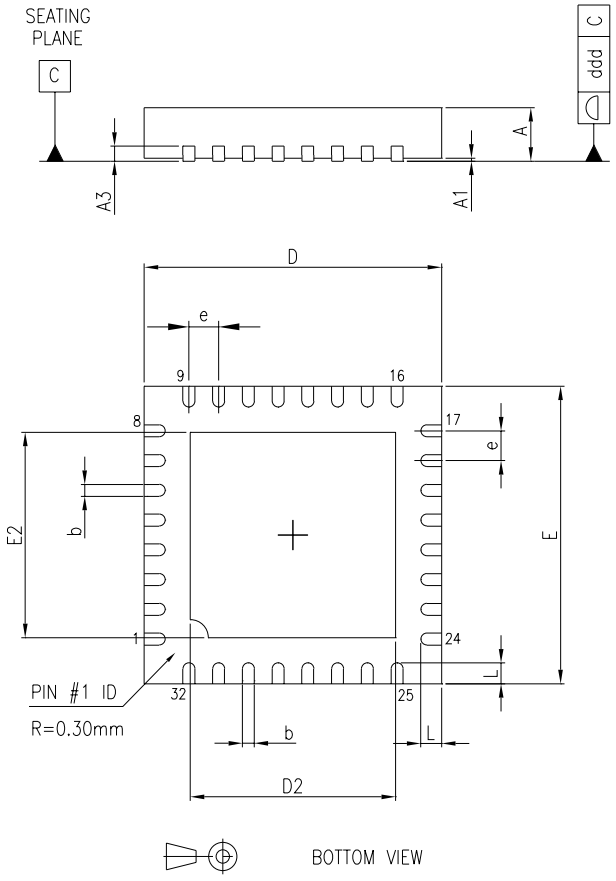
Table 12. QFN32 (5 x 5 mm) mechanical data

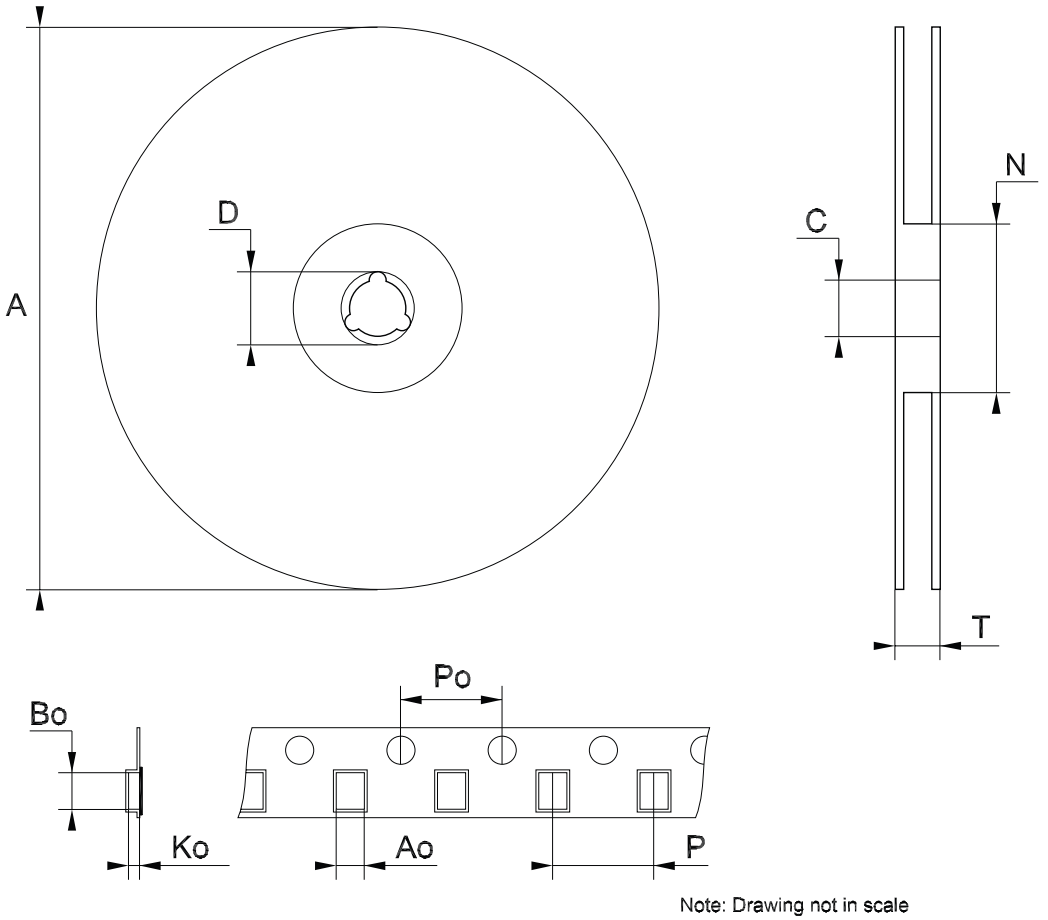
Dim.	(mm.)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2	3.20		3.70
E	4.85	5.00	5.15
E2	3.20		3.70
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 9. QFN32 package dimensions



Tape & reel QFNxx/DFNxx (5x5 mm.) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		5.25			0.207	
Bo		5.25			0.207	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

10 Revision history

Table 13. Document revision history

Date	Revision	Changes
03-Dec-2009	1	Initial release.
18-Mar-2010	2	Modified: *Figure 3 on page 11* and *Figure 5 on page 12*.

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